

Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

ln	Re	Application	of:
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Justin K. Brask et al. Fenty, Jesse A. Examiner:

U.S. Serial No: 10/750,061 Art Unit: 2815

Filed: December 30, 2003

For: NONPLANAR TRANSISTOR WITH

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Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450

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has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

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	37 C.F.R. §1.97(b).			
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If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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Dated: 12/22, 2004

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Substitute for Form 1449/PTO					Complete if Known		
	INICOD	ΝΛΛ.	TION DISCLOSUR	Application Number	10/750,061		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)					Filing Date	December 30, 2003	
					First Named Inventor:	Justin K. Brask et al.	
					Art Unit	2815	
	<u>ڇَ</u>			Examiner Name	Fenty, Jesse A.		
Street	LARY 1		of	2	Attorney Docket Number	42P16680	
TRAD			U.S. PATEN	T DOCUMENTS			
Examiner Initials*	er Cite No.1		Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant	
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		WO 02/43151A	5/30/2002	Hitachi ULSI Sys Co Ltd				

Examiner	Date	Considered	
Signature			

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SENT FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Substitute for Form 1449/PTO Complete if Known **Application Number** 10/750,061 INFORMATION DISCLOSURE Filing Date December 30, 2003 STATEMENT BY APPLICANT First Named Inventor: Justin K. Brask et al. (use as many sheets as necessary) Art Unit 2815 **Examiner Name** Fenty, Jesse A. Attorney Docket Number **Sheet** 2 of 2 42P16680 NON PATENT LITERATURE DOCUMENTS T² Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the Examiner Cite item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue No¹ Initials* number(s), publisher, city and/or country where published V. Subramanian et al., " A Bulk-Si-Compatible Ultrathin-body SOI Technology for Sub-100m MOSFETS" Proceeding of the 57th Annual Device Research Conference, pp. 28-29 (1999) Hisamoto et al., "A Folded-channel MOSFET for Deepsub-tenth Micron Era". 1998 IEEE International Electron Device Meeting Technical Digest, pp 1032-1034 (1998)Huang et al., "Sub 50-nm FinFET: PMOS", 1999 IEEE International Electron Device Meeting Technical Digest, pp 67-70 (1999) Auth et al., "Vertical, Fully-Depleted, Surroundings Gate MOSFETS On sub-0.1um Thick Silicon Pillars", 1996 54th Annual Device Research Conference Digest, pp 108-109 (1996) Hisamoto et al., "A Fully Depleted Lean-Channel Transistor (DELTA)-A Novel Vertical Ultrathin SOI MOSFET", IEEE Electron Device Letters, V. 11(1), pp36-38 (1990). Jong-Tae Park et al., "Pi-Gate SOI MOSFET" IEEE Electron Device Letters, Vol. 22, No. 8, August 2001, pages 405-406 Hisamoto, Digh et al. "FinFET- A Self-Aligned Double-Gate MOSFET Scalable to 20 nm". IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pages 2320-2325 International Search Report PCT/US 03/26242 International Search Report PCT/US 03/39727 International Search Report PCT/US 03/40320